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T.BELL
7-5-01

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:

Kinsman et al.

Serial No.: 09/538,684

Filed: March 30, 2000

For: VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES

Examiner: D. Graybill

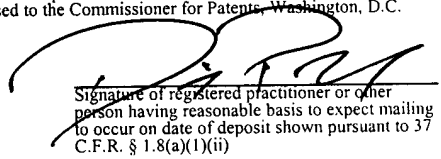
Group Art Unit: 2814

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AMENDMENT

Box NON-FEE AMENDMENT
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Sir:

This amendment is in response to the Office Action of March 20, 2001, whose initial period of response is set to expire on June 20, 2001.

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IN THE SPECIFICATION:

Please replace the first full paragraph on page 2 with the following:

Cross Reference to Related Applications: This application is a divisional of application

Serial No. 08/887,381, filed July 2, 1997, now United States Patent 6,159,764, issued

December 12, 2000. This application is related to a co-pending application entitled "LEAD

FRAME ASSEMBLIES WITH VOLTAGE REFERENCE PLANE AND IC PACKAGES

INCLUDING SAME," filed July 2, 1997, having Serial No. 08/888,336, now United States .

Patent 5,955,777, issued September 21, 1999, and commonly assigned with the present

application.

IN THE CLAIMS:

Cancel claims 5, 13, 30 and 38.

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

A marked-up copy of the amended claims is set forth in Appendix A attached hereto.

Please amend the claims as follows:

1. (Twice Amended) An integrated circuit (IC) package comprising:
a package body;
an IC die positioned within the package body;
a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and
an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the IC die, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

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B3

2. (Amended) The IC package of claim 1, wherein the package body is selected from a group consisting of a transfer molded plastic package body and a preformed ceramic package body.

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3. (Amended) The IC package of claim 1, wherein the IC die is selected from a group consisting of a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, and a processor IC die.

4. (Amended) The IC package of claim 1, wherein the lead frame is selected from a group consisting of a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

*SUB
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6. (Amended) The IC package of claim 1, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

NE

8. The IC package of claim 1, wherein the heat sink is positioned only partially within the package body.

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9. (Twice Amended) The IC package of claim 1, wherein the heat sink is coupled to a printed circuit board outside the package body thereby coupled to one of a signal voltage and a reference voltage.

10. The IC package of claim 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

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11. (Amended) The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

12. The IC package of claim 1, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

14. The IC package of claim 1, wherein the first and second portions of the heat sink are integral with one another.

15. The IC package of claim 1, wherein the first and second portions of the heat sink comprise separate parts.

NE
16. The IC package of claim 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. The IC package of claim 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. The IC package of claim 1, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

19. The IC package of claim 1, further comprising an adhesive attaching the lead frame to the heat sink.

20. The IC package of claim 1, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

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22. (Twice Amended) An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory

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devices, at least one of the input, output, memory, and processor devices including an integrated circuit (IC) package comprising:
a package body;
an IC die positioned within the package body;
a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and
an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and having a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink being opposite the die-attach area and projecting away from the first portion of the heat sink and the IC die.

*508
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C3*

24. (Twice Amended) An integrated circuit (IC) package comprising:
a package body;
an IC die positioned within the package body;
a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and
an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area of the plurality of leads of the lead frame, the die-attach surface being attached to the IC die.

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control

25. (Twice Amended) An integrated circuit (IC) package comprising:
an IC die;
a lead frame including a plurality of leads having portions that are connected to the IC die; and
an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the IC die, the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

26. (Amended) The IC package of claim 25, further comprising a package body.

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27. (Amended) The IC package of claim 26, wherein the package body is selected from a group consisting of a transfer molded plastic package body and a preformed ceramic package body.

28. (Amended) The IC package of claim 25, wherein the IC die is selected from a group consisting of a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, and a processor IC die.

29. (Amended) The IC package of claim 25, wherein the lead frame is selected from a group consisting of comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

B10 SUB C3
31. (Amended) The IC package of claim 25, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

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33. The IC package of claim 26, wherein the heat sink is positioned only partially within the package body.

SUB C3 B11
34. (Amended) The IC package of claim 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

NE
35. The IC package of claim 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

B12 SUB C3
36. (Amended) The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

NE
37. The IC package of claim 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

39. The IC package of claim 25, wherein the first and second portions of the heat sink are integral with one another.

40. The IC package of claim 25, wherein the first and second portions of the heat sink comprise separate parts.

41. The IC package of claim 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

NE
42. The IC package of claim 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. The IC package of claim 25, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

44. The IC package of claim 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. The IC package of claim 25, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

REMARKS

Claims 1 through 4, 7 through 12, 14 through 21, 22 through 29, 31 through 37, and 39 through 45 are currently pending in the application.

Claims 5, 13, 30, and 38 have been canceled.

Claims 7, 21, 23 and 32 are withdrawn from consideration as being directed to a non-elected species of invention in response to an Election of Species Restriction Requirement.

This amendment is in response to the Office Action of March 20, 2001.

Claims 2 through 4 and 27 through 29 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 1, 2, 4 through 6, 8 through 20, 24 through 27, 29 through 31 and 33 through 45 were rejected under 35 U.S.C. § 102(e) as being anticipated by Marrs (United States Patent 5,701,034).

Claims 3, 22 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Marrs (United States Patent 5,701,034) as applied to claims 1, 2, 4 through 6, 8 through 20, 24 through 27, 29 through 31 and 33 through 45 above, and further in combination with Wark (United States Patent 5,696,031).

Applicants have amended the claimed invention as suggested by the Examiner for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention in a proper Markush group language to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 2 through 4 and 27 through 29 are allowable under the provisions of 35 U.S.C. § 112.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turning to the Marrs reference, packaged semiconductor die 101 is connected to the leads 102 of a lead frame having a heat sink 110 underlying both portions of the leads of the lead frame and the die having one or more conductive layers 206 used as a ground plane, power plane, or for signal routing.

Applicants have amended claims 1, 2, 4 through 6, 8 through 20, 24 through 27, 29 through 31, and 33 through 45 to clearly distinguish over the Marrs reference under 35 U.S.C. § 102. As presently amended, independent claims 1, 22, 24, and 25 have been amended to include the element of the invention calling for “an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die”

Applicants submit that the Marrs reference does not and cannot anticipate the presently claimed invention of independent claims 1, 22, 24, and 25 as the element of the claimed invention calling for “an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die” is not, either expressly or inherently, described in as complete detail as is contained in the claimed invention in the Marrs reference.

Therefore, independent claims 1, 22, 24, and 25 are allowable as well as the dependent claims therefrom over the cited prior art under 35 U.S.C. § 102.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there

must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Turning to the Wark reference, a multi-chip module used in conjunction with a processor, an input device, and an output device.

Regarding the rejection of claims 3, 22, and 28 under 35 U.S.C. § 103, Applicants submit that neither the Marrs reference, nor the Wark reference, nor any combination of the Marrs reference and the Wark reference teach or suggest the limitations of the presently claimed invention calling for "an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die"

Furthermore, Applicants submit that any rejection of the presently claimed invention based upon any combination of the Marrs reference and the Wark reference would be a hindsight reconstruction of the claimed invention based solely upon the Applicants' disclosure as the cited prior art fails to teach or suggest all the elements and limitations of the presently claimed invention. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper.

Therefore, the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention.

Accordingly, claims 3, 22, and 28 are allowable over the cited prior art under 35 U.S.C. § 103.

In summary, Applicants submit that claims 1 through 4, 6, 8 through 12, 14 through 20, 22, 24 through 29, 31, 33 through 37, and 39 through 45 are clearly allowable over the cited prior art and clearly comply with the provisions of 35 U.S.C. § 112. Additionally, Applicants submit that claims 7 and 32 are allowable as depending from allowable independent claims.

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Applicants request the allowance of claims 1 through 4, 6, 7, 8 through 12, 14 through 20, 22, 24 through 29, 31, 32, 33 through 37, and 39 through 45 and the case passed for issue.

Respectfully submitted,



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